Otto-von-Guericke Universität Magdeburg
Arbeitsgruppe für Eingebettete Systeme und Betriebssysteme
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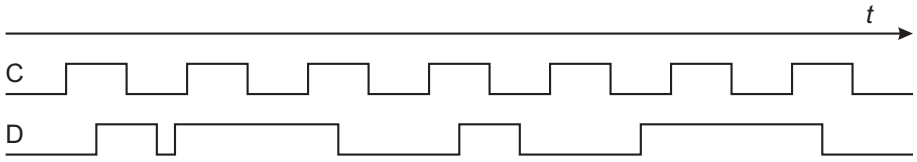
Theoretisches Aufgabenblatt 3

Abgabetermin: 10.11.-12.11.2012

1. Construct the time series of the output of a D-Flip-Flop. The input values follow the time series shown below. Assume a D-Flip-Flop which is:

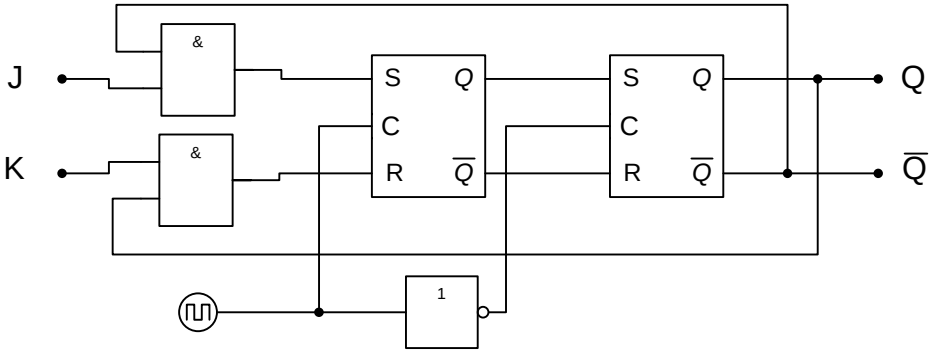
   a) level-triggered.
   b) positive-edge-triggered.
   c) negative-edge-triggered.
   d) master-slave.



2. Draw the circuit of a triggered RS-Flip-Flop using only
   a) NAND-Gates
   b) Nor-Gates

   and explain its working principle.

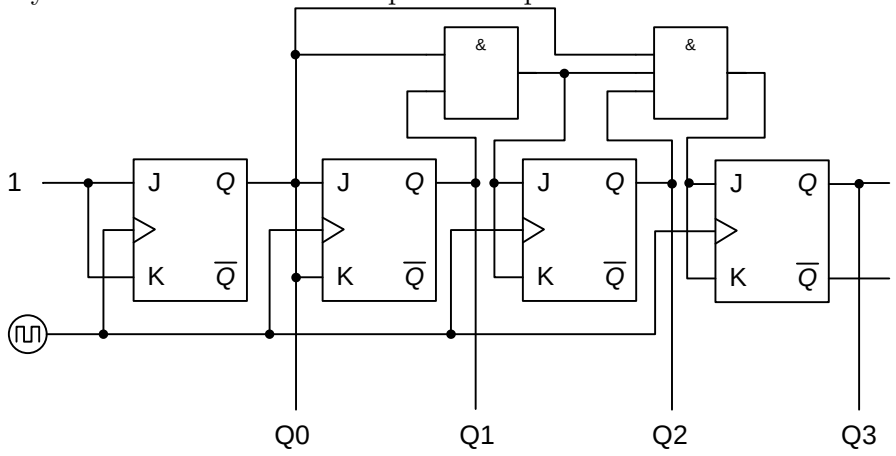
3. a) Which type of Flip-Flop is visible in the circuit shown below? What is the purpose of the AND-Gates at the inputs? What happens whenever $J = K = 1$? Why is a Master-Slave-Flip-Flop used? Why is a single Flip-Flop not enough?



   b) Complete the following truth table of a RS-Flip-Flop. Construct the boolean equation $Q_{n+1}(Q_n, S, R)$ and simplify it.

S	R	Q_n	Q_{n+1}	
0	0	0		
0	0	1		save
0	1	0		
0	1	1		reset
1	0	0		
1	0	1		set
1	1	0	x	
1	1	1	x	invalid

4. Analyse the following circuit. Which function(s) are implemented? Is it a synchronous or asynchronous circuit? Is a simplification possible?



5. Construct the circuit to control the floor light of house inhabited by multiple families. Whenever a floor light switch is used the and the lights are off, the lights should be switched on. Another use of any light switch shall then switch it off again.